## ABSTRACT OF THE DISCLOSURE

A delay optimization designing system and method is disclosed by which reduction of outputting delay and setup time of flip-flops and clock skew can be achieved and sufficient delay optimization can be achieved. A delay optimization designing system for a logic circuit includes a flip-flop selection section for selecting any flip-flop not to be substituted into a latch from within a given logic circuit, a flip-flop searching section for searching any flip-flop having a delay margin from among the flip-flops which are not selected by the flip-flop selection section, and a latch substitution section for substituting any flip-flop searched by the flip-flop searching section into a latch which passes a signal to the output side therethrough faster than the searched flip-flop.